LCRB I2C PROTOCOL

GENERAL DEFINITION

Target EBE device address: 0x33 per default. Read only.
I²C running in Standard Mode with max. clock speed of 100 kHz.

VIRTUAL REGISTER TABLE

The values are in big endian format (MSB first, LSB last).

REGISTER (HEX)	READ/WRITE	DATA TYPE	DESCRIPTION
0x00	read	32 bit signed	Level signal
0x04	read	32 bit signed	Reserved (output = 0x00 0x00 0x00 0x00)
0x08	read	32 bit signed	Temperature (range: -5000 up to +15000 = -50.00°C up to +150.00°C)
0x0c	read	32 bit signed	Reserved (output = 0x0F 0x0F 0x0F 0x0F)
0x10	read	8 bit signed	Reserved
0x11	read	8 bit unsigned	Sensor type: 0x4c resp. “L” for LCRB
0x12	read	8 bit unsigned	Reserved
0x12	read	8 bit unsigned	Reserved
0x14	Read	16 bit unsigned	Reserved
0x16	read	8 bit unsigned	Reserved
:	read	8 bit unsigned	Reserved
0x37	read	8 bit unsigned	Reserved

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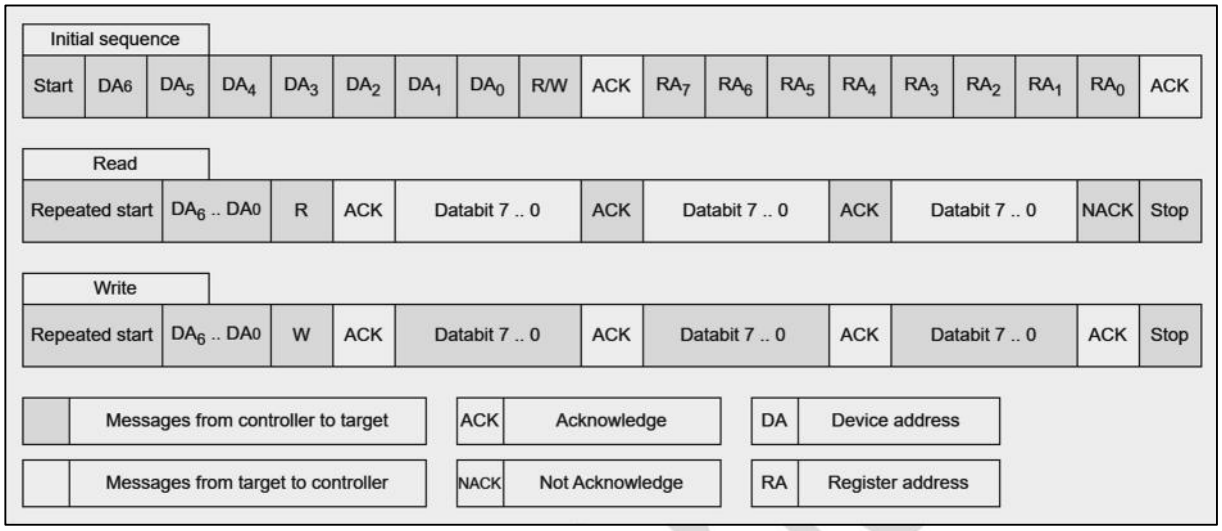
COMMUNICATION BETWEEN SENSOR AND CONTROLLER

For I²C communication between controller and target the combined format is used. Therefore an initial sequence followed with a different sequence depending on a reading or writing operation is applied which is shown in the following picture.



Initial sequence

The initial sequence begins with a start operation from the controller followed by the 7-bit long device address to whom the controller wants to communicate with. For the 8th-bit the controller transmits a “0” for a writing communication and “1” for a reading communication.
The target device sends an acknowledge bit (ACK) afterwards if the message is transmitted correctly – a not acknowledge bit (NACK) otherwise.
At the end of the initial sequence the controller sends the 8-bit long register address which is acknowledge by the target.

Read/Write sequence

The combined format applies another start condition. This allows the I²C bus to transmit several bytes of data without closing the connection between the controller and the target.
Followed by the device address and the equivalent read/write bit from the controller, the target acknowledges and the data transmission can be done.
Depending on a read or write communication, controller and target interplay 8-bit data followed by an ACK-bit. This can be done for several bytes.
The transmission ends when the controller sends a stop condition.

Note: The controller sends an NACK-bit after the last byte of data to end the transmission.

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Start and repeated start condition

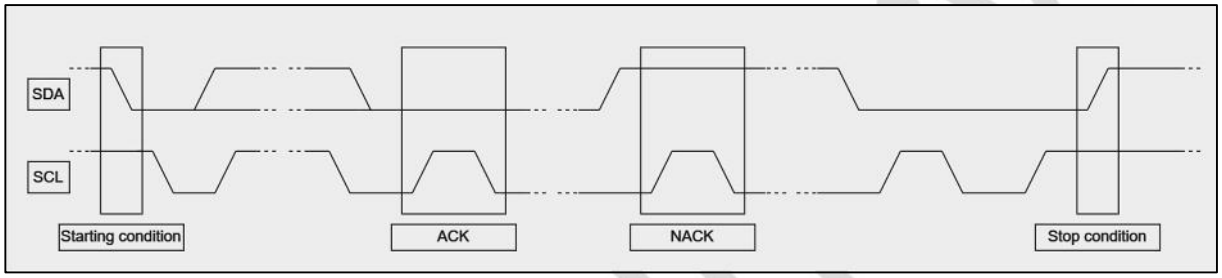
The SDA line switches from a high voltage level to a low voltage level before the SCL line switches from high to low.

Stop condition

The SDA line switches from a low voltage level to a high voltage level after the SCL line switches from low to high.

Acknowledge condition

After the transmission of every byte the target responds to the controller with the ninth bit whether the transmission was successful (ACK) or not (NACK).
The SDA line switches from a high voltage level to a low voltage level for an ACK.
The SDA line stays on a high voltage level for a NACK.



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DISCLAIMER

The information contained in this document is for general guidance only. The user is responsible for determining the suitability of the technical information referred to herein for his application. On delivery of the component, EBE is only obliged to implement those properties set out and agreed upon in this technical data sheet. Further properties are not included. No guarantee is given. The component has been designed for installation in our customer's products. Manufacturer of the resulting product and consequent liability according to the Product Liability Act lies with the customer.